CLAIMS

1. A method of forming a high voltage multiple output current device comprising:

providing a substrate of a first conductivity type;

forming a first doped region of a second conductivity type on a first portion of the substrate including forming the first doped region as a first closed geometric shape having a center and a first periphery wherein a first portion of the first periphery has a first contour and a second portion of the first periphery has a second contour and also wherein the first doped region includes a drain and a source of a J-FET transistor, a drain of a first MOS transistor, and a drain of a second MOS transistor;

forming on the substrate a second doped region of the second conductivity type having a second periphery wherein a portion of the second periphery is juxtaposed to the first portion of the first periphery and has a third contour that is shaped the same as the first contour and wherein the second doped region is a source of the first MOS transistor; and

forming on the substrate a third doped region of the second conductivity type having a third periphery wherein a portion of the third periphery is juxtaposed to the second portion of the first periphery and has a fourth contour that is shaped the same as the second contour and wherein the third doped region is a source of the second MOS transistor.

2. The method of claim 1 further including forming a gate of the first MOS transistor overlying a portion of the first portion of the first periphery and the portion of the second periphery wherein a portion of the gate of the first MOS transistor has a fifth contour that is

shaped the same as the first contour, and forming a gate of the second MOS transistor overlying a portion of the second portion of the first periphery and the portion of the third periphery wherein a portion of the gate of the second MOS transistor has a sixth contour that is the same shape as the second contour.

3. The method of claim 1 wherein forming the first doped region of the second conductivity type on the first portion the substrate including forming the first doped region as the first closed geometric shape having the center and the first periphery includes forming the first doped region as a circle having a first radius from the center.

4. The method of claim 3 wherein forming on the substrate the second doped region and forming on the substrate the third doped region includes forming the second doped region as a first arc of a circle having a second radius from the center and forming the third doped region as a second arc of a circle having a third radius from the center.

5. The method of claim 1 further including forming a fourth doped region of the second conductivity type within the first doped region.

6. The method of claim 1 further including forming a first resistor having a first terminal coupled to the first doped region and a second terminal coupled to the second doped region.

7. The method of claim 1 further including forming a second resistor having a first terminal coupled to the first doped region and a second terminal coupled to the third doped region.

8. A high voltage multiple output current device comprising:

a substrate of a first conductivity type;

a first doped region of a second conductivity type on a first portion the substrate, the first doped region formed as a first closed geometric shape having a center and a first periphery wherein a first portion of the first periphery has a first contour and a second portion of the first periphery has a second contour and also wherein the first doped region is a drain and a source of a J-FET transistor, a drain of a first MOS transistor, and a drain of a second MOS transistor;

a second doped region of the second conductivity type on the substrate and having a second periphery wherein a portion of the second periphery is juxtaposed to the first portion of the first periphery and has a third contour that is the same shape as the first contour wherein the second doped region is a source of the first MOS transistor; and

a third doped region of the second conductivity type on the substrate and having a third periphery wherein a portion of the third periphery is juxtaposed to the second portion of the first periphery and has a fourth contour that is the same shape as the second contour, and wherein the third doped region is a source of the second MOS transistor.

9. The high voltage multiple output current device of claim 8 further including a first gate structure overlying a portion of the first portion of the first periphery and the second periphery, and also including a second gate structure overlying a portion of the second portion of the first periphery and the third periphery.

10. The high voltage multiple output current device of claim 8 further including a fourth doped region of the second conductivity type within the first doped region, the fourth doped region having a heavier doping than the first doped region.

11. The high voltage multiple output current device of claim 8 further including a low on-resistance transistor coupled to receive current from the first MOS transistor and responsively conduct an ESD to a voltage return.

12. The high voltage multiple output current device of claim 11 wherein the low on-resistance transistor is also coupled to the drain of the J-FET transistor.

13. The high voltage multiple output current device of claim 11 further including an operating voltage detector having an input coupled to receive an output voltage of the second MOS transistor and to disable the second MOS transistor when the output voltage is equal to or greater than a desired value.

14. The high voltage multiple output current device of claim 11 further including a first current control loop coupled to receive current from the third doped region of the second conductivity type, the first current control loop having an output; a second current control loop coupled to receive current from the second doped region of the second conductivity type, the second current control loop having an output; and a capacitor coupled to the output of the first and second current control loops.

15. The high voltage multiple output current device of claim 14 further including an operating voltage detector having an input coupled to the output of the first current control loop to receive an output voltage of the first and second current control loops and to disable the first MOS transistor and the second MOS transistor when the output voltage is equal to or greater than a desired value.

16. The high voltage multiple output current device of claim 15 further including an inhibit transistor coupled to the output of the first current control loop to couple current from the second MOS transistor to a voltage return.

17. A power control system inhibition method comprising:

generating a first output current at an output of a system controller responsive to a first value of an output voltage; and

coupling the output to a voltage return to inhibit generation of the first output current.

18. The method of claim 17 further including generating a second output current at the output of the system controller responsively to a second value of the output voltage wherein the second output current is less than the first output current.

19. The method of claim 18 wherein generating the second output current includes generating both the first output current and the second output current when the output voltage is greater than the first value, and disabling generating the first output current and the second output current when the output voltage is at least equal to a third value wherein the first value is greater than the second value, and the third value is greater than both the first value and the second value.

20. The power control system inhibition method of claim 17 further including receiving an input voltage on an input of the system controller, generating the first output current, charging a capacitor coupled to the output with the first output current, and disabling the first output current when the output voltage is a second value that is greater than the first value.